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09/838,461	04/19/2001	Richard James Eickemeyer	AUS920000649US1	2096

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EXAMINER

O'BRIEN, BARRY J

ART UNIT PAPER NUMBER

2183

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/838,461

Applicant(s)

EICKEMEYER ET AL.

Examiner

Barry J. O'Brien

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 07 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-13, 20 and 21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13, 20 and 21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. Claims 1-13, 20 and 21 have been examined.

#### ***Papers Submitted***

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as received on 7/07/2004.

#### ***Drawings***

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “thread control signals sent to the hold latches being delayed in time from the thread control signals sent to the register file”, as in claims 1, 7 and 13, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement

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Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Specification*

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

### *Claim Rejections - 35 USC § 112*

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

8. Claim 1 recites the limitation, “one of the thread control signals, applied to the hold latches, is delayed in time from another of the thread control signals, applied to the multithreaded register file, when selecting the thread to thereby accommodate pipelining of instructions by the multithreading processor”. However, the Specification only describes that the control signals are applied in a delayed fashion, and makes no mention of the delaying of the signals “accommodating” pipelining of instructions (see p.9 of the Specification). Thus, the Specification has not conveyed that the Applicant had possession of the claimed invention at the time the application was filed. Also see claims 7 and 13, which contain the same un-described claim language, and thus are rejected for the same reasons as claim 1. Dependent claims 2-6, 8-13 and 20-21 contain all the limitations of their respective parent claims, and thus are rejected for the same reasons as above.

9. Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

10. Claim 1 recites the limitation, “one of the thread control signals, applied to the hold latches, is delayed in time from another of the thread control signals, applied to the multithreaded register file, when selecting the thread to thereby accommodate pipelining of instructions by the multithreading processor”. However, the Specification has not described how one of ordinary skill in the art would make a pipeline that accommodates pipelining to delaying control signals. Thus, the Specification has not enabled one of ordinary skill in the art to make or use the invention as claimed without undue experimentation. Also see claims 7 and 13, which contain

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the same un-described claim language, and thus are rejected for the same reasons as claim 1.

Dependent claims 2-6, 8-13 and 20-21 contain all the limitations of their respective parent claims, and thus are rejected for the same reasons as above.

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-5, 7-11, 13 and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Joy et al., U.S. Patent No. 6,341,347.

13. Regarding claims 1 and 7, taking claim 7 as exemplary, Joy has taught a data processing system, comprising:

- a. A memory unit (see Col.20 lines 1-9),
- b. A mixed-mode multithreading processor (902 of Fig.9, also see Col.18 lines 39-52),
- c. A bus coupling the mixed-mode multithreading processor to the memory unit (see Fig.9 and Col.20 lines 1-9),
- d. Wherein the mixed-mode multithreading processor comprises:
  - I. A thread control unit (610 of Fig.6),

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- II. A multithreaded register file having a plurality of registers (see Fig.13, also see Col.8 lines 27-44),
- III. A plurality of hold latches (434/444 of Fig.4B, also see Col.10 lines 38-64 and Col.11 lines 48-67),
- IV. Wherein each of a plurality of the registers in the multithreaded register file and each of a plurality of the hold latches stores data representing a first instruction thread and a second instruction thread (see Col.11 lines 48-67 and Col.27 lines 26-38),
- V. The thread control unit provides thread control signals to said hold latches (see Col.11 lines 48-67) and registers (see Col.8 lines 27-44) selecting a thread using said thread control signals (see Col.15 line 52 – Col.16 line 9), wherein one of the thread control signals, applied to the hold latches, is delayed in time from another of the thread control signals, applied to the multithreaded register file, when selecting the thread to thereby accommodate pipelining of instructions by the mixed-mode multithreading processor (see Col.17 lines 19-32). Here, there is inherently a delay between when the thread control signal is applied to the hold latches and when it is applied to the register file. Joy has taught that the thread select signal is broadcast similar to how a clock signal is distributed (see Col.17 lines 27-32), and clock signals of different lengths and properties require synchronization by inserting delays (for example, see Denny et al., U.S. Patent No. 6,621,882, Col.1 lines 46-58). Because

the specification has not provided a reason for the delay between the two signals (see above paragraphs 7-10, as well as p.9 of the specification), it is inherent that delay must be introduced to synchronize the thread select signals, as they are of different length and properties and thus require synchronization.

14. Claim 1 is nearly identical to claim 7, differing in its lack of a memory unit and a bus, but encompassing the same scope as claim 7. Therefore, claim 1 is rejected for the same reasons as claim 7.

15. Regarding claims 2 and 8, taking claim 8 as exemplary, Joy has taught the data processing system as recited in claim 7, wherein the thread control unit via the thread control signals places at least one of the plurality of the hold latches and at least one of the plurality of the registers into an interleaving multithreading mode (see Col.17 lines 19-32). Here, because the thread ID signal (control signal) is supplied to both the registers and the hold latches (see Col.8 lines 27-44 and Col.11 lines 48-67), and because the thread controller can place the processor into a mode that outputs a thread ID based on interleaving using a thread timer (see Col.17 lines 19-32), the hold latches and the registers are inherently placed in interleaving mode.

16. Claim 2 is nearly identical to claim 8, differing in its parent claim, but encompassing the same scope as claim 8. Therefore, claim 2 is rejected for the same reasons as claim 8.

17. Regarding claims 3 and 9, taking claim 9 as exemplary, Joy has taught the data processing system as recited in claim 7, wherein the thread control unit, responsive to a determination that a latency in an instruction exceeding a first predetermined time has occurred in one of the two threads, sends control signals to said hold latches and register for reading out

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data exclusively from the other of the two threads until a second predetermined time has elapsed mode (see Col.17 lines 19-32). Here, the thread controller is operable to switch threads on both long-latency events such as cache misses, as well as on a thread timer signal, it is inherent that if a thread switch occurs due to a long latency event, and that if the thread timer expires before another long latency event causes a thread switch, then the processor will operate only on instructions, and use data from one set of registers/latches, until the timer expires.

18. Claim 3 is nearly identical to claim 9, differing in its parent claim, but encompassing the same scope as claim 9. Therefore, claim 3 is rejected for the same reasons as claim 9.

19. Regarding claims 4 and 10, taking claim 10 as exemplary, Joy has taught the data processing system as recited in claim 9, wherein the thread control unit returns said hold latches and registers to an interleaving multithreading mode after the expiration of the second time period (see Col.17 lines 19-32). Here, because the thread controller can place the processor into a mode that outputs a thread ID based on interleaving using a thread timer (see Col.17 lines 19-32), the hold latches and the registers are inherently placed in interleaving mode if no long-latency event has occurred since the previous long-latency event caused a thread switch.

20. Claim 4 is nearly identical to claim 10, differing in its parent claim, but encompassing the same scope as claim 10. Therefore, claim 4 is rejected for the same reasons as claim 10.

21. Regarding claims 5 and 11, taking claim 11 as exemplary, Joy has taught the data processing system as recited in claim 9, wherein the latency in an instruction exceeding a first predetermined time results from a load instruction that misses in a data cache (see Col.17 lines 19-32).

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22. Claim 5 is nearly identical to claim 11, differing in its parent claim, but encompassing the same scope as claim 11. Therefore, claim 5 is rejected for the same reasons as claim 11.

23. Regarding claim 13, Joy has taught the data processing system as recited in claim 7, wherein the mixed-mode multithreading processor is a first mixed-mode multithreading processor (see Col.18 lines 39-52), the thread control unit is a first thread control unit, the hold latches are first hold latches, the multithreaded register file is a first multithreaded register file, the plurality of registers are a plurality of first registers, and the data is a first data, and further comprising:

- a. A second mixed-mode multithreading processor (904 of Fig.9, also see Col.18 lines 39-52), wherein the second mixed-mode multithreading processor comprises:
  - I. A second thread control unit (610 of Fig.6),
  - II. A second multithreaded register file having a plurality of second registers (see Fig.13, also see Col.8 lines 27-44),
  - III. A plurality of second hold latches (434/444 of Fig.4B, also see Col.10 lines 38-64 and Col.11 lines 48-67),
  - IV. Wherein each of a plurality of the second registers and each of a plurality of the second hold latches stores second data representing a third instruction thread and a fourth instruction thread (see Col.11 lines 48-67 and Col.27 lines 26-38),
  - V. The second thread control unit provides second thread control signals to said second hold latches (see Col.11 lines 48-67) and second registers (see

Col.8 lines 27-44) selecting a second thread using said second thread control signals (see Col.15 line 52 – Col.16 line 9), wherein one of the second thread control signals, applied to the second hold latches, is delayed in time from another of the second thread control signals, applied to the second multithreaded register file, when selecting the second thread to thereby accommodate pipelining of second instructions by the second mixed-mode multithreading processor (see Col.17 lines 19-32). Here, there is inherently a delay between when the thread control signal is applied to the hold latches and when it is applied to the register file. Joy has taught that the thread select signal is broadcast similar to how a clock signal is distributed (see Col.17 lines 27-32), and clock signals of different lengths and properties require synchronization by inserting delays (for example, see Denny et al., U.S. Patent No. 6,621,882, Col.1 lines 46-58). Because the specification has not provided a reason for the delay between the two signals (see above paragraphs 7-10, as well as p.9 of the specification), it is inherent that delay must be introduced to synchronize the thread select signals, as they are of different length and properties and thus require synchronization.

24. Regarding claims 20 and 21, taking claim 21 as exemplary, Joy has taught the data processing system as recited in claim 7, further comprising a plurality of flow through latches (434/444 of Fig.4B, also see Col.10 lines 38-64 and Col.11 lines 48-67) used to break multiple-

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cycle paths into distinct stages of a pipeline for pipelining the instructions (see Col.12 lines 1-19).

25. Claim 20 is nearly identical to claim 21, differing in its parent claim, but encompassing the same scope as claim 21. Therefore, claim 20 is rejected for the same reasons as claim 21.

***Claim Rejections - 35 USC § 103***

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

27. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joy et al., U.S. Patent No. 6,341,347, as applied to claims 3 and 9, respectively, above, and further in view of Kalafatis et al., U.S. Patent No. 6,535,905.

28. Regarding claims 6 and 12, taking claim 12 as exemplary, Joy has taught the data processing system as recited in claim 9, wherein the latency in an instruction exceeding a first predetermined time results from a long latency operation such as a cache miss or interrupt request (see Col.17 lines 19-32).

29. Joy has not explicitly taught wherein the long latency event is a mispredicted branch.

30. However, Kalafatis has taught performing a thread switch in response to long latency events, including a mispredicted branch and cache misses (see Kalafatis, Col.13 lines 47-53) so that idle clock cycles can be avoided and processor performance can be increased (see Kalafatis, Col.1 lines 12-31). Therefore, one of ordinary skill in the art would have found it obvious to

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modify the processor of Joy to also perform thread switching on a long-latency branch misprediction so that processor performance can be improved.

31. Claim 6 is nearly identical to claim 12, differing in its parent claim, but encompassing the same scope as claim 12. Therefore, claim 6 is rejected for the same reasons as claim 12.

### ***Response to Arguments***

32. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. After October 12<sup>th</sup>, 2004, the examiner can be reached at (571) 272-4171. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm, with the exception of first Friday of every bi-week.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached at (703) 305-9712, or at (571) 272-4162 on or after October 12<sup>th</sup>, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

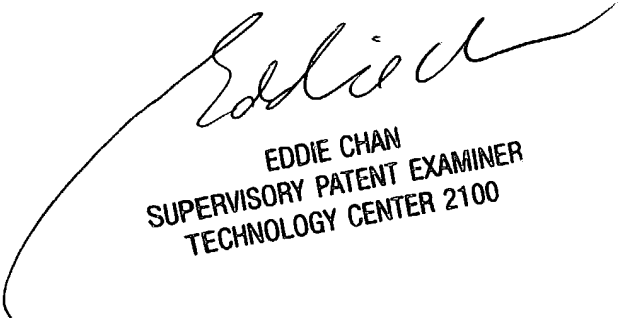
36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien  
Examiner  
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